

AUG 20 2007

PTOL-413A (09-04)

Approved for use through 07/31/2005. OMB 0651-0031  
U.S. Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

## Applicant Initiated Interview Request Form

Application No.: 10/840,125 First Named Applicant: Ting  
 Examiner: Crane, Sara W. Art Unit: 2811 Status of Application: Final Rejection

## Tentative Participants:

(1) Mary Adams-Moe (2) \_\_\_\_\_  
 (3) \_\_\_\_\_ (4) \_\_\_\_\_

Proposed Date of Interview: 8/23/07Proposed Time: 3:00 (AM/PM)  
Eastern

## Type of Interview Requested:

(1) ☒ Telephonic (2) ☐ Personal (3) ☐ Video Conference

Exhibit To Be Shown or Demonstrated: ☐ YES ☐ NO

If yes, provide brief description: \_\_\_\_\_

## Issues To Be Discussed

Issues (Rej., Obj., etc)	Claims/ Fig. #s	Prior Art	Discussed	Agreed	Not Agreed
(1) <u>New matter objection</u>			<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
(2) <u>112 rejection</u>			<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
(3) _____			<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
(4) _____			<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
<input type="checkbox"/> Continuation Sheet Attached					

## Brief Description of Arguments to be Presented:

All matter was included in Specification as filed.

An interview was conducted on the above-identified application on \_\_\_\_\_

NOTE: This form should be completed by applicant and submitted to the examiner in advance of the interview (see MPEP § 713.01).

This application will not be delayed from issue because of applicant's failure to submit a written record of this interview. Therefore, applicant is advised to file a statement of the substance of this interview (37 CFR 1.133(b)) as soon as possible.

Mary Adams-Moe  
Applicant/Applicant's Representative Signature\_\_\_\_\_  
Examiner/SPE SignatureMary Adams-Moe  
Typed/Printed Name of Applicant or Representative57883  
Registration Number, if applicable

This collection of information is required by 37 CFR 1.133. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 21 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

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**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

In re application:	§	
Notched Spacer for CMOS transistors.	§	
	§	
Application No.: 10/840,125	§	Group Art Unit: 2811
	§	
Filed: 05/06/2004	§	Examiner: Crane, Sara W
	§	
Inventor:	§	Attorney Docket No.:
Steve Ming Ting	§	TSM03-0945
	§	

**AGENDA FOR TELEPHONE INTERVIEW**

Dear Examiner Crane,

I would like to schedule a phone interview with you concerning application number 10/840,125. I have recently been assigned this file. I would like to propose the following amendments as discussion points.

**Paragraph 25**

As illustrated in FIG. 1e, the portion of the first dielectric layer 126 (FIG. 1d) located under the notched-spacer masks 130 is removed due to the isotropic etch process, thereby creating a notched spacer. The width of the notch will be dependent upon the thickness of the first dielectric layer 126 and the notch height may be controlled by varying the etch duration. Furthermore, FIG. 1e illustrates the situation in which the first dielectric layer 126 is removed completely to the gate electrode 122. In other situations, the portion of the first dielectric layer 126, located under the notched-spacer masks 130 may remain on the side of the gate electrode 122, because of the inherent property of the isotropic etch to clear the thickest portion of dielectric layer 126 last. This Leaving a thin dielectric layer 126 on the lower portion of the side of the gate electrode 122 may be desirable, for example, when it is preferred to control the depth and angle of the implant or to protect the gate electrode 122 or gate dielectric 120 from damage during the etching process or other processes.

**Claim 16**

A method of forming a semiconductor device, the method comprising:

forming a gate electrode on a substrate, the substrate having a first conductivity type;

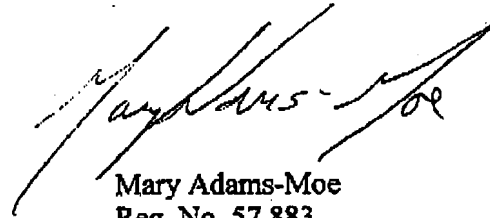
forming a notched spacer comprised of a single homogenous layer alongside the gate electrode, wherein a lower portion of the notched spacer is thinner than an upper portion of the notched spacer;

performing a first ion implant wherein only the gate electrode and the notched spacer act as masks during the first ion implant, the first ion implant using ions of the first conductivity type; and

performing one or more second ion implants using ions of a second conductivity type.

The afternoon of **Thursday 8/23 at 3:00 pm** Eastern time is the best time for me, however, I will adjust my schedule to anytime that is convenient for you. Please confirm our appointment or suggest a new time.

Thank-you,  
Best Regards,  
Mary



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